

ASYNCHRONOUS AUTOMATA IMPLEMENTATION USING ONLY LOGIC GATES

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Abstract: The use of asynchronous sequential circuits has brought many advantages to system development, given the following examples:

- Signal interface protocols (for example SCSI)
- Asynchronous circuits are ideal for building modular systems. This modular structure enables a global system time checkup. The asynchronous circuits developed for high performance systems, for speeds up to 75 MHz, function correctly for lower speeds also. An asynchronous sequential system can be built from a number of modules, by interfacing them.

1.INTRODUCTION

Asynchronous circuits are hard to implement because of the hazard, caused by different glitches that can appear in different parts of the system. Unlike the synchronous systems, the asynchronous ones cannot tolerate glitches, because they are very sensitive regarding every change in state or input variables. That is why care must be taken in advance by analyzing different hazard types.

A asynchronous sequential system does not contain a clock signal for synchronization. Every part of the system synchronizes locally with neighboring circuits. This deters clock slew periods. As it was mentioned before, in order to reduce power consumption, CMOS circuits are used, because the power requirements for them are lower in idle mode.

Some recent implementations show the potential of systems implemented using asynchronous circuits:

- 80C51 is a full asynchronous microcontroller implemented by Philips Research and Philips Semiconductor [1]; the system consumes only a fourth of the power consumed by a corresponding synchronous system. This microcontroller can be found in some pagers produced by Philips.
- A asynchronous instruction decoder, produced by Intel, whose performance is boosted 3,4 times that the synchronous counterpart [2].
- Amulet2e circuit, a microprocessor produced by the Manchester University [3]. This includes an asynchronous ARM processor with level 1 cache. It has better performance than in synchronous variant, the dissipated power being 1 microwatt when the processor is in idle state.
- A digital filter, part of a synchronous sequential system used for hearing aid, was implemented totally asynchronous by the Dutch Technical University and Oticon, Inc. [4]. The asynchronous system dissipates five times less power than the synchronous system.
- RISC processor, based on MIPS-X architecture [5].

Other examples include: a asynchronous sequential system used for solving equations [1], asynchronous processor [4], Reed-Solomon error detector used in digital audio systems [5], high performance divisor circuit[16], infrared communications processor [3], parallel processing router processor [2].

Although synchronous sequential systems are widely spread, there is a series of applications that deter their use:

- The circuit has input variables that can change at any given time and cannot be synchronized with the clock signal
- If a system is complex enough and the time response of the logic elements is low, it can be hard to assure that the clock signal propagates simultaneously to all the flip-flops
- The applications has to be fast enough and the system cannot tolerate loss of time due to the clock wait states

In such cases, the use of asynchronous sequential system is required. They are not synchronized by a general clock signal; when an input modifies, the state of the circuit may change almost instantaneously.

- All impulse inputs must have a minimum time period, in order to command flip-flops
- The time interval between two successive impulses must be long enough for the system to respond accordingly.

2. DESIGN OF AN ASYNCHRONOUS MACHINE

The architecture of a sequential system is illustrated in figure 1. The “n” notation means current time variables and “n+1” means the time after the variable is changed. The “ \triangle ” notation refers to delay circuits.

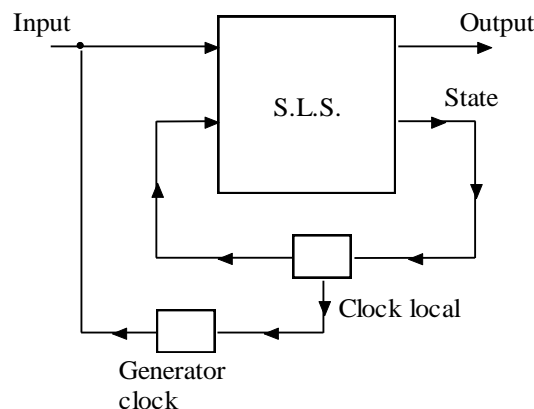


Figure 1. Asynchronous machine

Binary arrays are defined as follows:

- Input $X = \{ x_{p-1}, x_{p-2}, \dots, x_0 \}$
- State $Y = \{ y_{N-1}, y_{N-2}, \dots, y_0 \}$
- Output $Z = \{ z_{q-1}, z_{q-2}, \dots, z_0 \}$

The system variables have the following dependencies:

$$Y_{j,n+1} = f_j(x_{p-1,n}; x_{p-2,n}; \dots; x_{0,n}; y_{N-1,n}; y_{N-2,n}; \dots; y_{0,n}) \text{ with } 0 \leq j \leq N - 1 \text{ and}$$

$$Z_{k,n+1} = g_k(x_{p-1,n}; x_{p-2,n}; \dots; x_{0,n}; y_{N-1,n}; y_{N-2,n}; \dots; y_{0,n}) \text{ with } 0 \leq k \leq q - 1$$

The following notation is used: $F = \{ f_{N-1}, \dots, f_0 \}$; $G = \{ g_{q-1}, \dots, g_0 \}$

Using the last two notations the Mealy machine can be represented by vector equations, figure 2.

$$\begin{aligned} Y_{N+1} &= F(X_n, Y_n) \\ Z_n &= G(X_n, Y_n) \end{aligned} \quad (1)$$

The Moore machine is similar to the Mealy, with the following equation:

$$\begin{aligned} Y_{N+1} &= F(X_n, Y_n) \\ Z_n &= G(Y_n) \end{aligned} \quad (2)$$

A Moore machine, figure 2 has the output vector dependent only on the state variables. The following terms will be used next:

- Transition table (Veitch-Karnaugh table for $y_{i,n+1}$ variables)
- Output table (Veitch_Karnaugh table for $z_{k,n}$ variables)
- State table
- State diagram

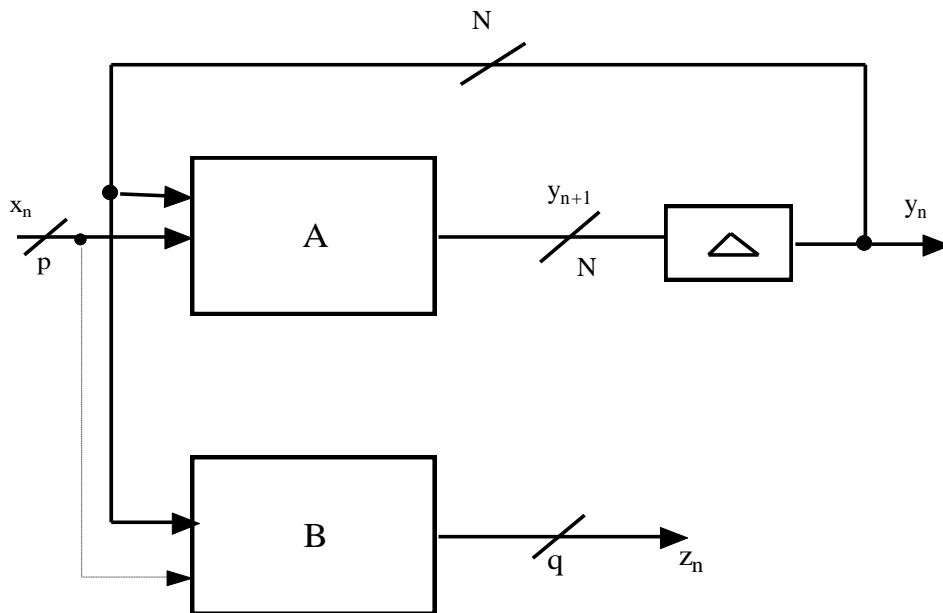


Figure 2. Moore/Mealy machine

3. ASYNCHRONOUS SEQUENTIAL SYSTEM SYNTHESIS USING ELEMENTARY LOGIC CIRCUITS

The synthesis of a sequential system is proposed as it follows. The system generates a impulse z after the low-high transition of the H signal, figure 3.

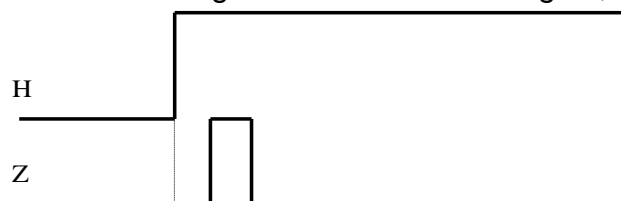


Figure 3. Timing diagram signal

The state diagram based on the time diagram is shown in figure 4.

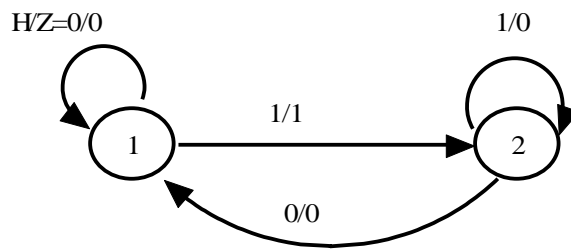


Figure 4. Fluence graph table

The following equations are deduced:

$$\begin{aligned} y_{n+1} &= H_n \\ z_n &= \overline{y_n} H_n \end{aligned} \quad (3)$$

Because there must be a minimum delay between the y_n and y_{n+1} variables, a RC circuit is used like the one in figure 5.

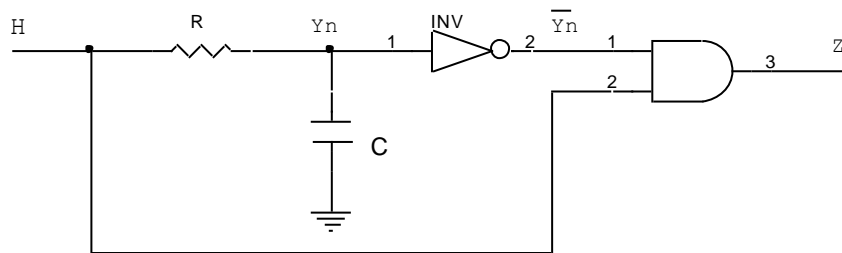


Figure 5. RC circuit

The signal diagram is presented in figure 6. The z signal duration is proportional to the RC constant of the circuit.

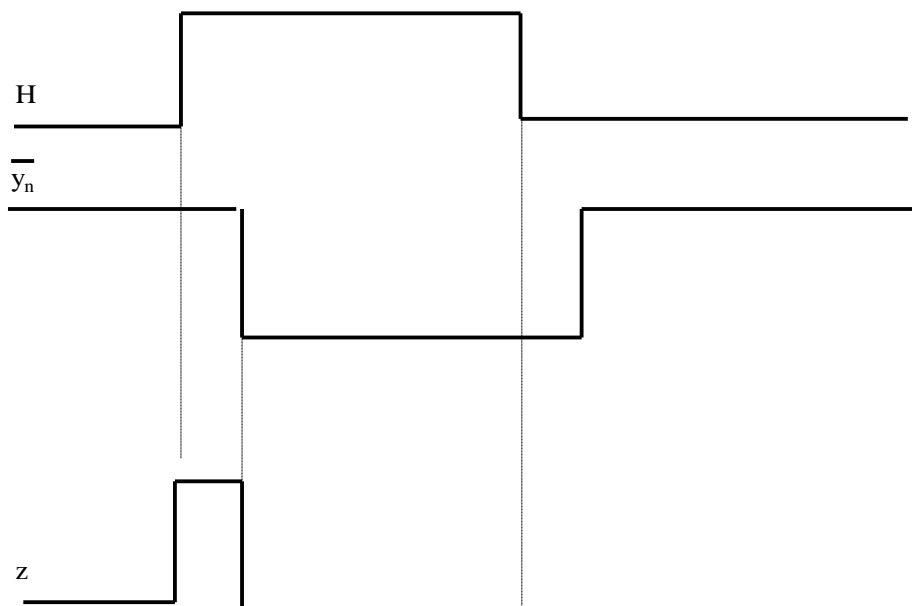


Figure 6. State diagram signal

The system implemented only with logic gates is presented in figure 7.

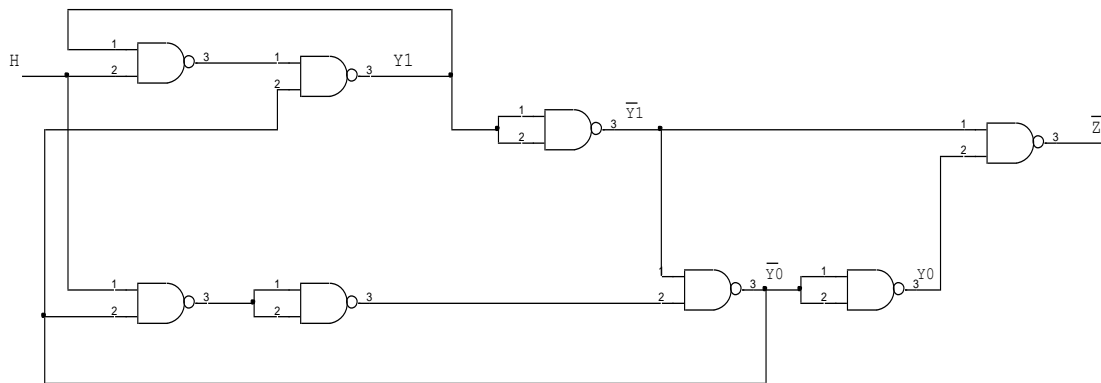


Figure 7. Implementation of asynchronous machine

If we assume that the t_{pLH} , t_{pHL} periods are equal, a partial signal diagram is presented in figure 8.

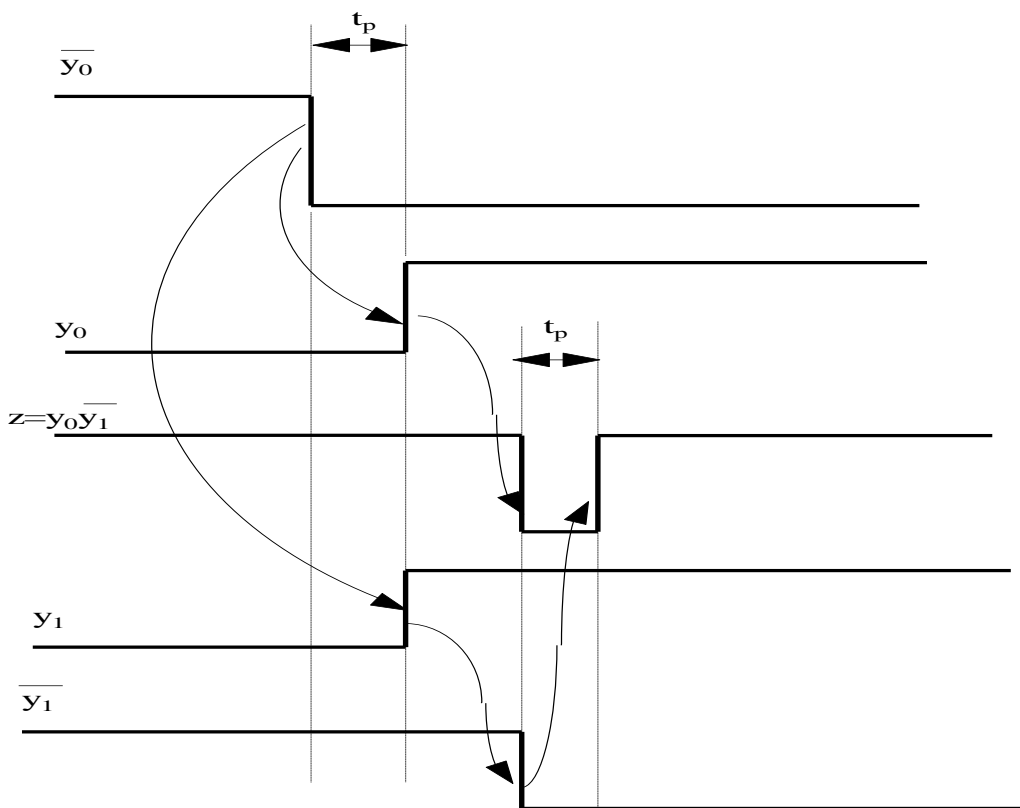


Figure 8. Signal diagram

The z signal duration is equal to t_{pLH} , t_{pHL} , so is unacceptable to command other circuits.

4. CONCLUSIONS

The design of asynchronous circuit is more difficult than the design of synchronous ones considering the propagation delay of signal trough elementary circuits. To simplify the analysis and the design of asynchronous systems, their operation is considered to be in fundamental mode. Operating in fundamental mode means that the input signals can change their state only if the circuit is in a stable state, meaning that no state variable is

modifying. In fundamental mode all inputs are considered to be levels. Sometimes there is considered the impulse mode, where the inputs can provide impulses (level variations).

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